ENGN 2912k Final Project

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For my final project, I designed an Analog to Digital Converter for robotic control systems applications. This converter was designed to sample the output of an angle sensor that senses the angular position of a controller. An example application for this sensor and ADC pair could be to sense the turning of a steering wheel for a basic robotic or automotive system.

I. Target Specifications

I chose Infineon's TLE5x09A16(D) Analog AMR/GMR Angle Sensor[1] for this application because of its high accuracy. For control and navigation of robotic systems, it is important to have a precise means for determining angular position; therefore, one of my primary specifications was to have a very high-precision angle sensor and a high-resolution ADC that would be able to appropriately measure the sensor's analog output. The sensor is automotive qualified, which means that the measured angle's error is small enough for the desired application.

This sensor contains an Anti-isotropic Magneto-Resistive (AMR) component with a 180-degree angle measurement capability and a Giant Magneto-Resistive (GMR) component with a 360-degree angle measurement capability for redundancy. Each sensor has four voltage outputs: positive cosine, negative cosine, positive sine, and negative sine. I chose to use the positive cosine and positive sine outputs of the AMR sensor for this project for simplicity, such that the chip will be used in the single-ended (and not differential) mode. The positive cosine output will be referred to as V_{sin}, and the positive sine output will be referred to as V_{cos}. Both V_{sin} and V_{cos} have an angle error of 0.1 degrees.

Number of Bits

In order to preserve the preciseness of the angle sensor measurement, I constrained the quantization error to be around the same size as the noise error for the sensor circuit. The output-referred RMS noise of the sensor circuit is 5 mV_{RMS}.

The definitions for the least significant bit voltage of the ADC (q, Equation 1) and RMS quantization error ($e_{q\,RMS}$, Equation 2) yield a definition of quantization error dependent on the full scale voltage ($V_{FS} = V_{dd}$) and number of bits (N).

$$q = \frac{V_{FS}}{2^N - 1} \quad (1)$$

$$e_{q\,RMS} = \frac{q}{\sqrt{12}} \quad (2)$$

$$e_{q\,RMS} = \frac{V_{FS}}{\sqrt{12}(2^N - 1)} \quad (3)$$

Setting the quantization error equal to the noise error,

$$\frac{V_{FS}}{\sqrt{12}(2^N - 1)} = 5 * 10^{-3}\, V_{RMS}$$

[1] https://www.infineon.com/dgdl/Infineon-TLE5x09A16_D-DS-v02_00-EN.pdf?fileId=5546d462696dbf12016977889fe858c9

$$N = \log_2 \frac{V_{FS} + 5 * 10^{-3} * \sqrt{12}}{5 * 10^{-3} * \sqrt{12}}$$

$N = 7.5814$ bits for $V_{FS} = 3.3V$

Sampling frequency requirement

Since the sensor's angle measurement can be up to 0.1 degrees, I required that sampling must be often enough to detect a 0.1-degree change. For automotive applications, the maximum steering wheel speed is estimated to be around 120 revolutions per minute[2]. From these values, the minimum period component in the measured Vsin and Vcos signals can be determined.

$$T_{min} = 0.1\ degrees * \frac{1\ revolution}{360\ degrees} * \frac{1\ minute}{120\ revolutions} * \frac{60\ seconds}{1\ minute} = 0.0001389\ s$$

Since T = 1/f, the maximum frequency (f_s) can be determined.

$$f_{max} = \frac{1}{T_{min}} = 7200\ Hz = 7.2\ kHz$$

The sigma-delta ADC was selected for this application due to its noise shaping characteristics that allow for reduced noise in the sampling bandwidth. For sigma-delta ADCs, the Signal-to-Noise Ratio (SNR) can be characterized by Equation 4[3].

$$SNR = 10\log_{10}\sigma_x^2 - 10\log_{10}\sigma_e^2 - \log_{10}\frac{\pi^2}{3} + 30\log_{10}\frac{f_s}{2f_{max}} \quad (4)$$

Where σ_x^2 = input signal variance

σ_e^2 = noise error variance

f_s = sampling frequency

It is important to note that the sampling frequency is not equal to the Nyquist frequency ($2f_{max}$) for sigma-delta ADCs; these ADCs use oversampling and thus require a much larger sampling rate than the Nyquist sampling ADCs.

Since the desired number of bits is 7.58 bits for V_{dd} = 3.3V, the desired SNR can be determined to be 47.4 dB by Equation 5.

$$SNR = 6.02 * N + 1.76\ dB \quad (5)$$

For the desired full-scale sinusoidal input, Equation 6 defines variance.

$$\sigma_x^2 = \frac{(V_{FS}/2)^2}{2} \quad (6)$$

Additionally, σ_e^2 can be defined in terms of V_{FS} and N_{ADC}, as shown in Equation 7. This N_{ADC} is not the resolution of the output signal (N): it is the resolution of the internal ADC and DAC within the sigma-delta ADC. For this project, N will be 1 for simplicity of design, allowing for the use of a 1-bit ADC and 1-bit DAC in the ADC implementation.

$$\sigma_e^2 = {e_q}_{RMS}^2 = \frac{(V_{FS}/(2^{N_{ADC}}-1))^2}{12} \quad (7)$$

Using equations 4, 6, and 7, with SNR = 47.4 dB, V_{FS} = 3.3V and N_{ADC} = 1, it can be determined that $f_s = f_{max} * 98.73 = 7.2kHz * 98.73 = 710.85\ kHz = 0.71085\ MHz$.

Table 1 summarizes the design targets and requirements for the ADC.

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[2] https://www.crossco.com/wp-content/uploads/2020/02/eaton-steering-catalog-sizing-and-application.pdf

[3] https://ieeexplore.ieee.org/document/482138

Table 1. *Overall ADC Design Requirements*

Parameter	Units	Requirement
ADC Type		Delta Sigma ADC
V_{DD}	V	3.3
Equivalent Number of Bits	bits	7.58 = 8
Power	J	Optimized to be low, but not primary constraint
Minimum Oversampling frequency	kHz	710.85

II. Design Methods

Sampling Circuit

The first stage of the ADC is a simple sample-and-hold circuit composed of a capacitor and a pass-transistor gate that samples the input waveform (vin). This clock switches at the oversampling rate, such that the signal is oversampled prior to modulation. This frequency was initially set to 710.84 kHz, which is the minimum required oversampling frequency. However, it was later increased to 2.86 MHz to enable functionality of the ADC. The value of the capacitor (1nF) was chosen experimentally such that it was sufficiently large to sample the input waveform.

Delta-Sigma Modulator

I first outlined the design for the analog part of the delta-sigma ADC. The basic components of the modulator are a summing circuit, an integrator, a comparator (ADC), a latch, and a feedback element (DAC)[4]. As described in the Target Specifications section, this modulator was designed to use an internal 1-bit ADC and 1-bit DAC. The ideal schematic for the modulator is shown in Figure 1.

The input to the modulator is the sum of the output of the sampling circuit and the feedback element. The first stage of the modulator is the integrator (op-amp) with output vint. The second stage is the comparator (op-amp) with output vcomp, which is connected to the third stage, which is a latch (D-Flip Flop) with output vout. Vout is the input to the last stage, which contains the feedback element with output vfb. The output of the modulator is the output of the latch. This is connected to a digital converter, which will be described in detail in the next section.

The modulator was first built and tested using ideal op-amps (Figure 1) and then later modified to use real, transistor-based op-amps (Figure 2). For this initial, ideal schematic, voltage-controlled voltage sources with a gain of 1000 were used. After initial testing using these ideal op amps was completed, I developed an operational amplifier from Johns & Martin's *Current Mirror op-amp with wide-swing cascode current mirrors* schematic (Figure 3). I biased the NMOS and PMOS transistors with vb1 and vb2, respectively, such that they were on and in saturation. The transistors were sized by setting all lengths to the same variable and setting the width of each corresponding pair (eg: M5 and M6 or M9 and M10) to the same variable to maintain differential symmetry. Then, a parametric sweep was performed to identify the transistor widths and length that allowed for high op-amp gain. The target gain was

[4] https://ieeexplore.ieee.org/document/5383302

1000 V/V (60 dB), since this gain was used for the ideal op-amps. The final sizes (Figure 3) resulted in an op-amp gain of 66 dB, f_{-3dB} = 19 kHz, and GBW = 37 MHz (Figure 4).

Digital Converter

Next, I made the digital logic part of the ADC which takes in the output of the delta-sigma modulator and generates a digital, 8-bit output (Figure 5). All digital logic was created using 0.5um transistor technology in order to match the 3.3V V_{DD} requirement for the angle sensor. The digital logic component of the ADC involved the use and design of an 8-bit counter (Figure 10), 9-bit counter, 8-bit register (Figure 9), and D-Flip-Flops (Figure 7). These digital components were created in a hierarchical manner using J-K Flip flops (Figure 8), D-Flip flops, 2-input and 3-input NAND gates, and inverters. The J-K and D Flip Flops were themselves composed of 2-input and 3-input NAND gates and inverters (Figure 6).

The inverted output of the delta-sigma modulator's flip flop is NAND-ed with the inverse of the oversampling clock to create a gated clock output. The gated clock was then put into a 8-bit counter, which counts how many times the gated clock transitions. The counter's CLEAR signal goes low (clearing the count) once 2^8 clock cycles have passed. This signal stays low for 4 clock cycles to ensure that the counter resets; the value of 4 clock CLEAR cycles was experimentally determined, since shorter CLEAR signals failed to properly clear and reset the counter. The 8 output bits of this counter are the inputs to an 8-bit register, which updates the ADC's outputs (Q0 to Q7) when the CLEAR signal initially goes low.

The CLEAR signal is generated by a 9-bit counter (pulse generator), which sets its MSB to 1 approximately when 2^8 cycles have passed. The output of this pulse generator is connected to two D-Flip Flops, which are each clocked by slowed-down versions of the original clock. The inverted output of the last flip flop is the CLEAR signal to the pulse generator, which resets it. This configuration allows the 9-bit counter it to work as a 2^8-cycle pulse generator with a pulse width of 4 cycles.

Figures 11 and 12 show the final implemented delta-sigma ADC schematic and corresponding testbench.

Figure 1. *Ideal Sampler and Modulator Schematic*

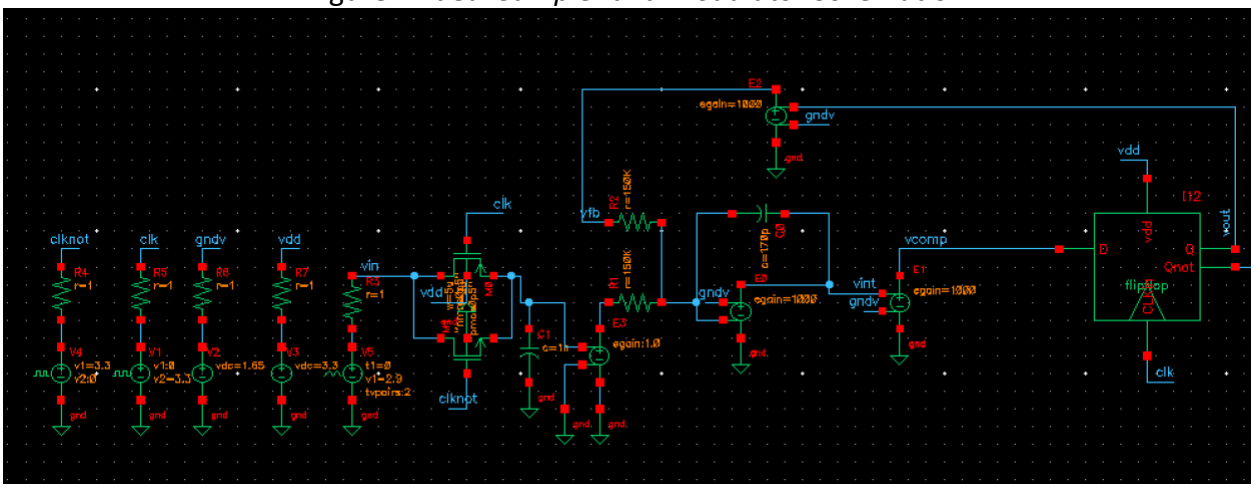


Figure 2. *Nonideal Sampler and Modulator Schematic*

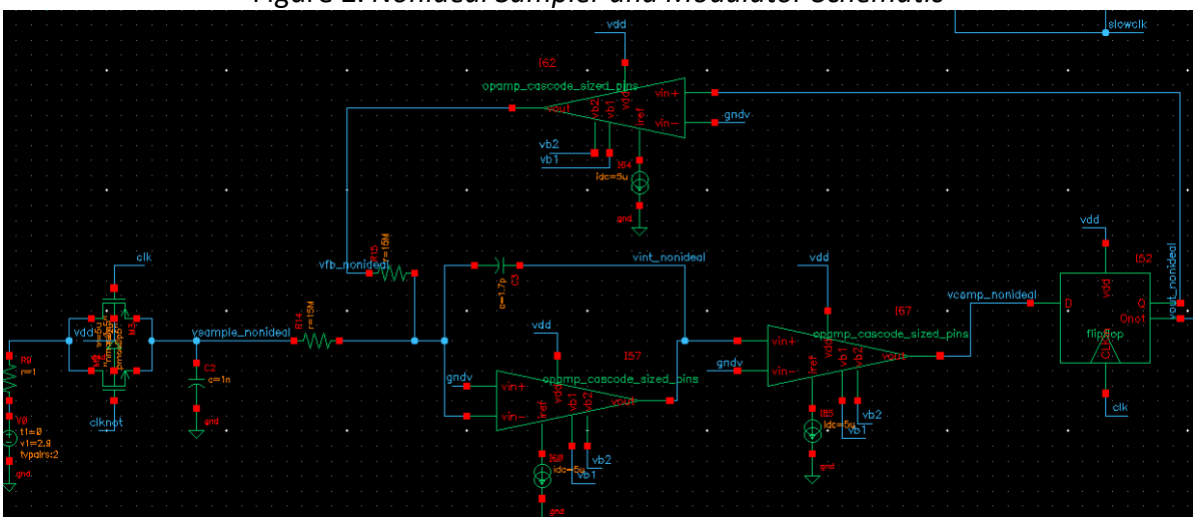


Figure 3. *Op Amp Schematic.*

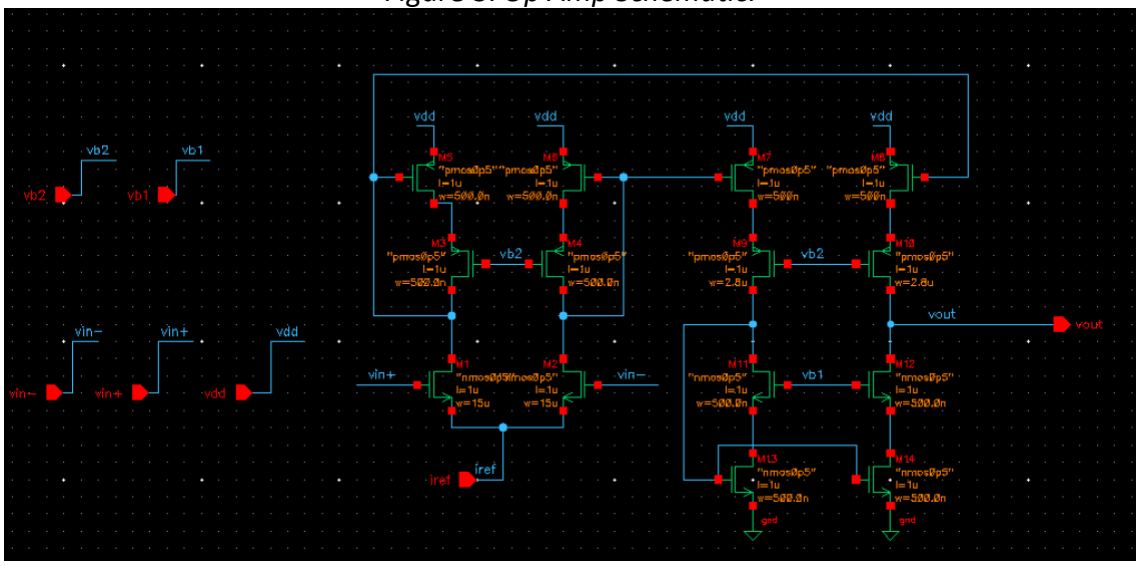


Figure 4. *Op amp frequency response*

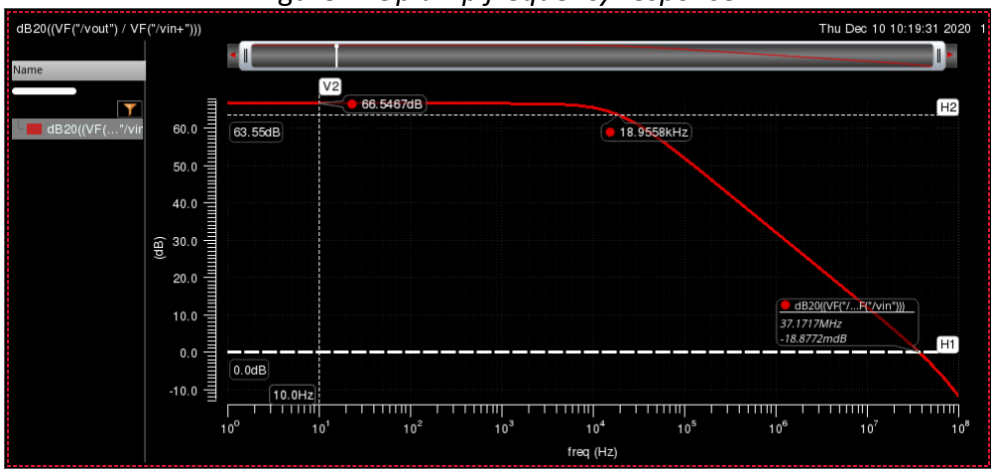


Figure 5. *Digital Converter Schematic*

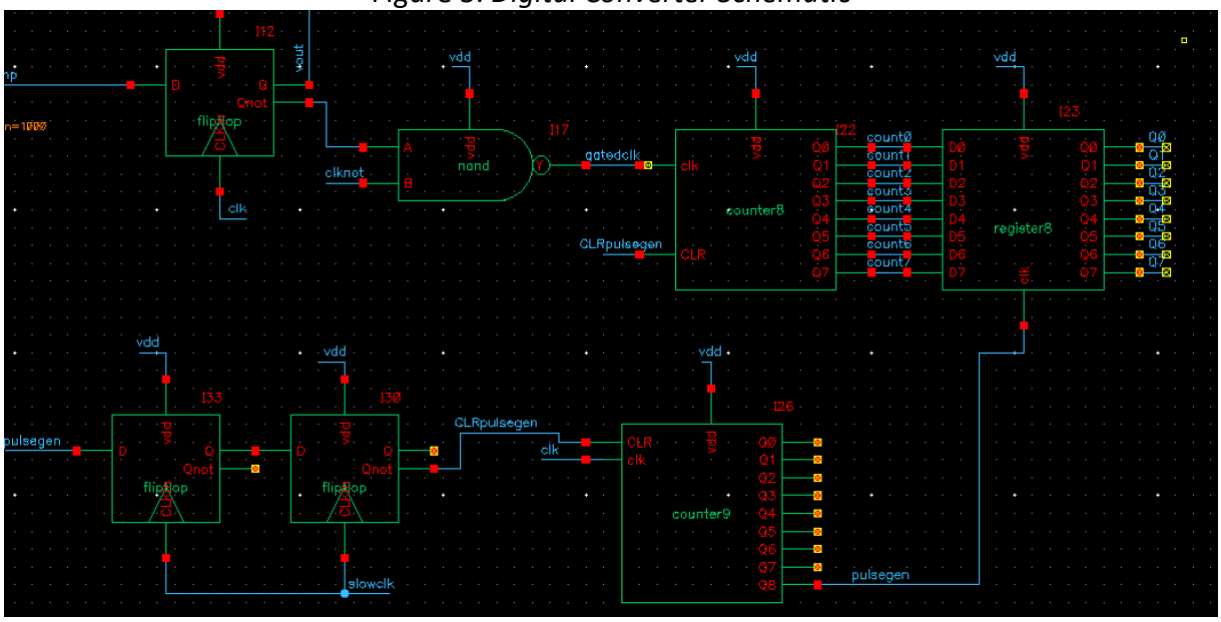


Figure 6*. 2-input (Left) and 3-input (Center) NAND and Inverter (Right) Schematics*

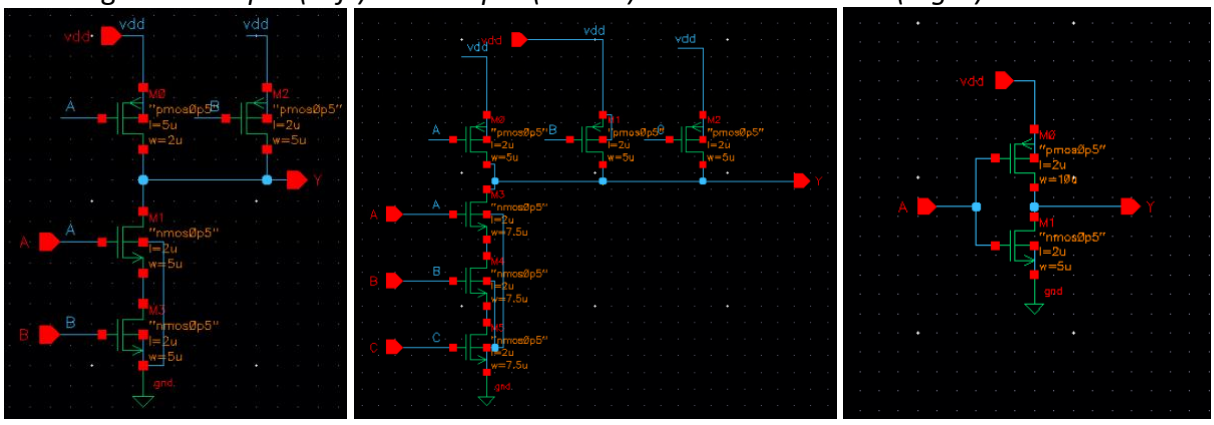


Figure 7. *D-Flip Flop Schematic*

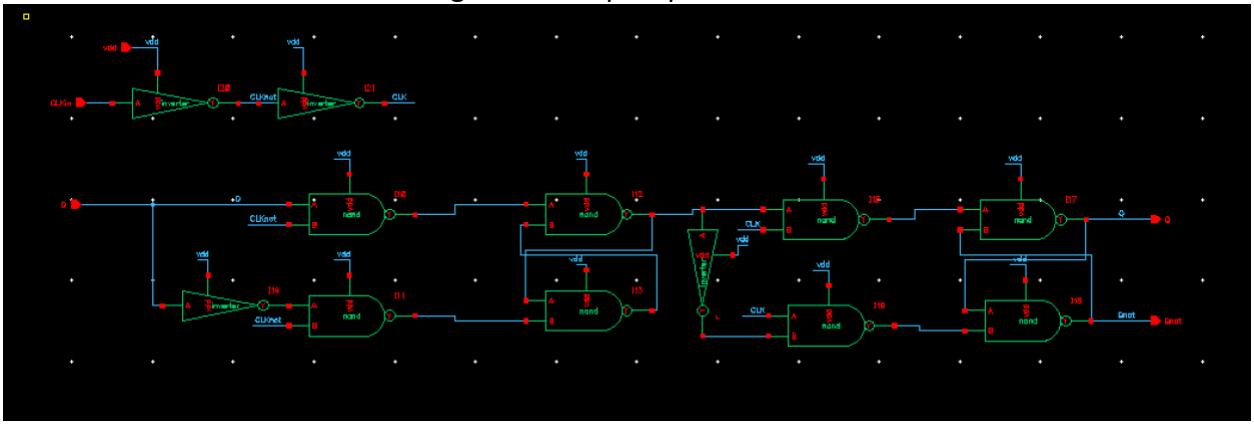


Figure 8. *J-K Flip Flop Schematic*

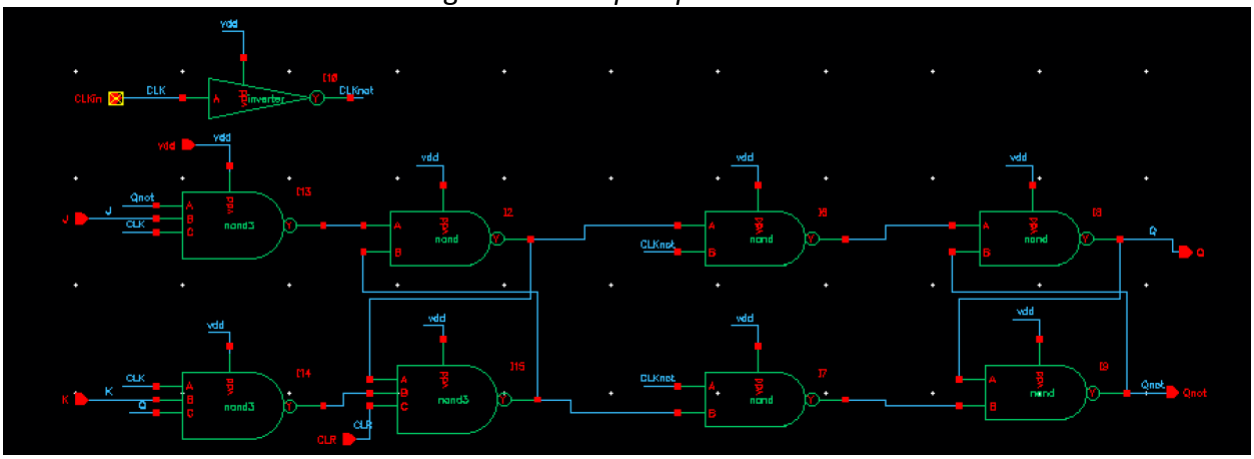


Figure 9. *8-bit Register Schematic (Top) and Zoomed in Schematic (Bottom)*

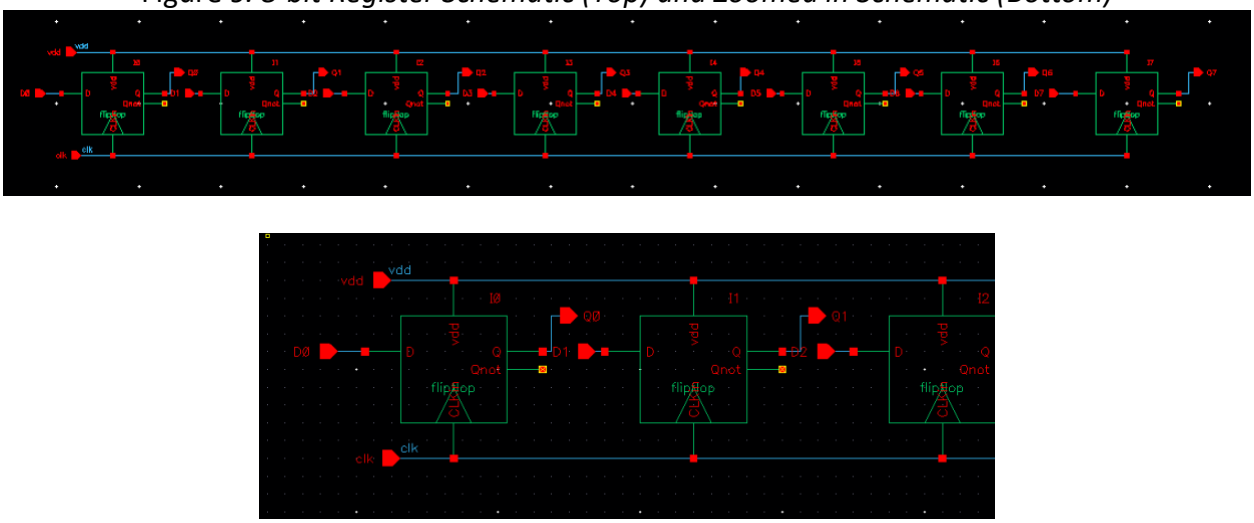
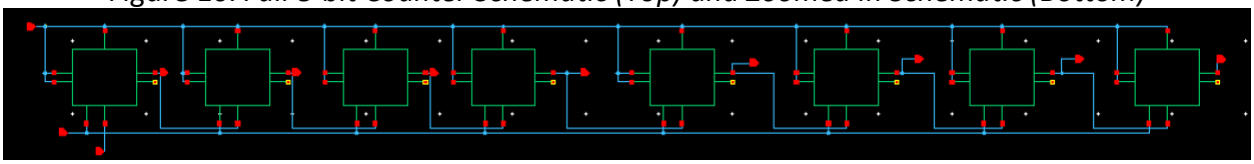


Figure 10. *Full 8-bit Counter Schematic (Top) and Zoomed in Schematic (Bottom)*



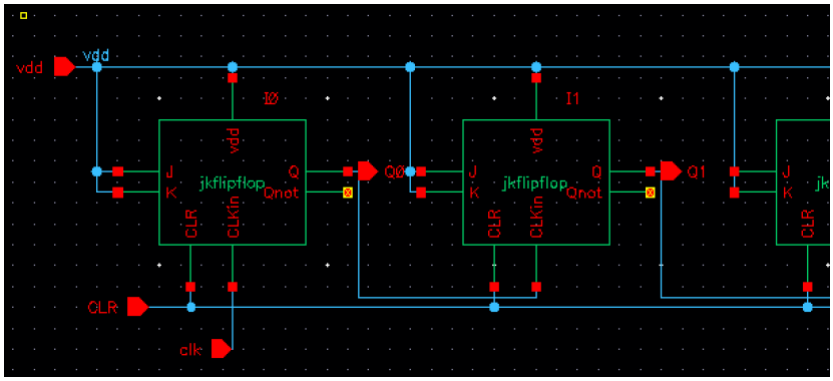


Figure 11. *Final Delta-Sigma Modulator Schematic*

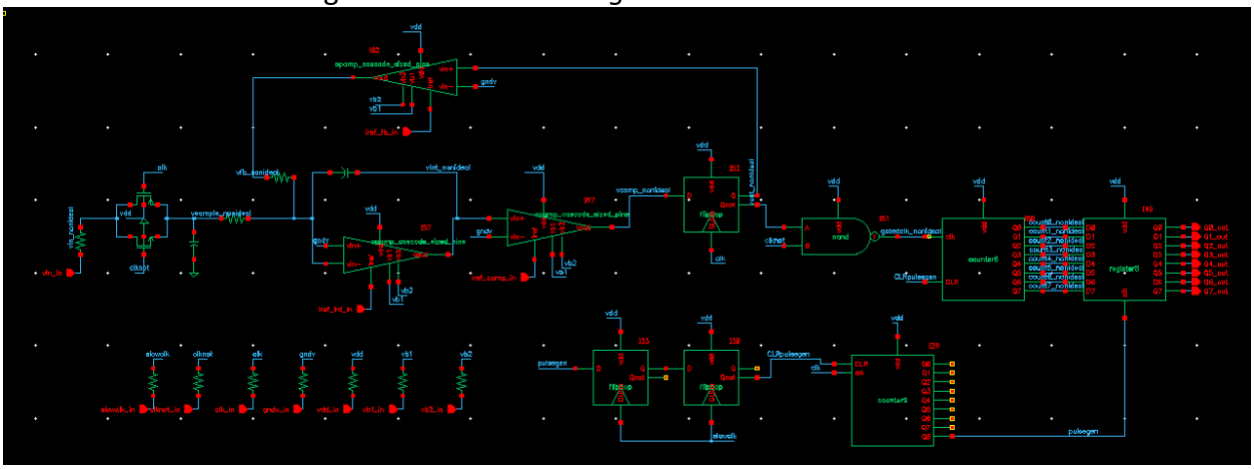
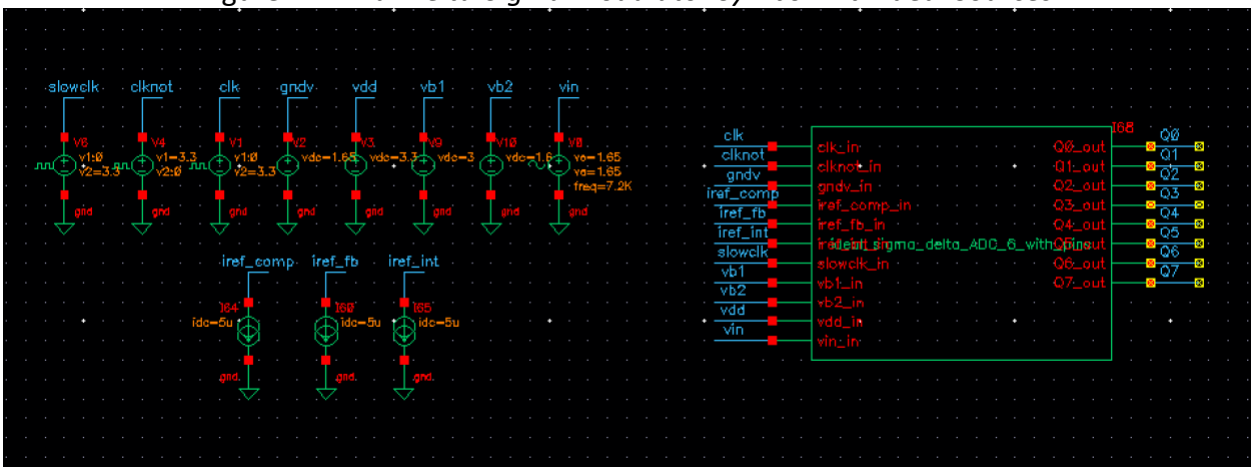


Figure 12. *Final Delta-Sigma Modulator Symbol with Ideal Sources*



III. Testing

Simulation Plots

The ADC was tested by applying a 2.9V to 3V voltage ramp to the input of the circuit. A transient simulation was then run to examine the ADC's digital outputs in response to this ramp. One transient simulation plot of the digital outputs of the ideal sigma-delta ADC (Figure 13) is shown, and a second shows the digital outputs of the nonideal ADC (Figure 14).

It is important to note that the first two digital outputs of the ADC must always be disregarded. The first output is always all zeroes due to the nature of the sampling circuit. Every time you get a new digital output from the circuit, this digital output reflects the average of the input signal during the sampling period that just happened. Therefore, during the first sampling cycle, no output value can be displayed.

The second output is invalid because of the sampling and modulating circuit propagation delay. When the input signal is first applied (prior to t=16 µs in Figure 15) where the modulator experiences irregular behavior such that the output of the modulator never goes high. This results in an effective delay, which deflates the count recorded by the digital output of the ADC. In future iterations of this ADC, the digital output of the ADC could be clocked using

a signal that accounts for this initial delay; this would make the second digital output valid. However, it is sufficient to ignore this value, and wait for subsequent outputs because they do not have this period where the output of the modulator is forced to zero.

The desired digital output for the ramp is a sequence of adjacent codes. For this particular ramp, both the ideal and nonideal ADCs begin counting at 226 and count up to 229. The ideal ADC does not skip any codes, while the nonideal ADC skips code 228. This discrepancy can be attributed to nonideal frequency response of the op-amps used in the nonideal ADC. However, the nonideal ADC still generally exhibits the expected trend for this the ramp input and has values very similar to the ideal ADC.

Figure 15 shows the internal signals of the nonideal delta-sigma modulator and compares the output of the integrator for the ideal and nonideal modulators (vint and vint_nonideal, respectively). The similarity between the two traces (in slope and general behavior) demonstrates the semi-ideal functionality of the nonideal op-amp, but the slight offset may contribute to errors, such as the aforementioned code skip.

Additional ramp tests of the final nonideal ADC are shown Figures 16 and 17. The test shown in Figure 14 shows the ADC output response to a 0.9 to 1V ramp over 1 ms, while Figure 15 shows the output response to a 2.5 to 2.6V ramp.

Figure 13. *ADC Output for Ideal Sampler and Modulator for 2.9 to 3V input*

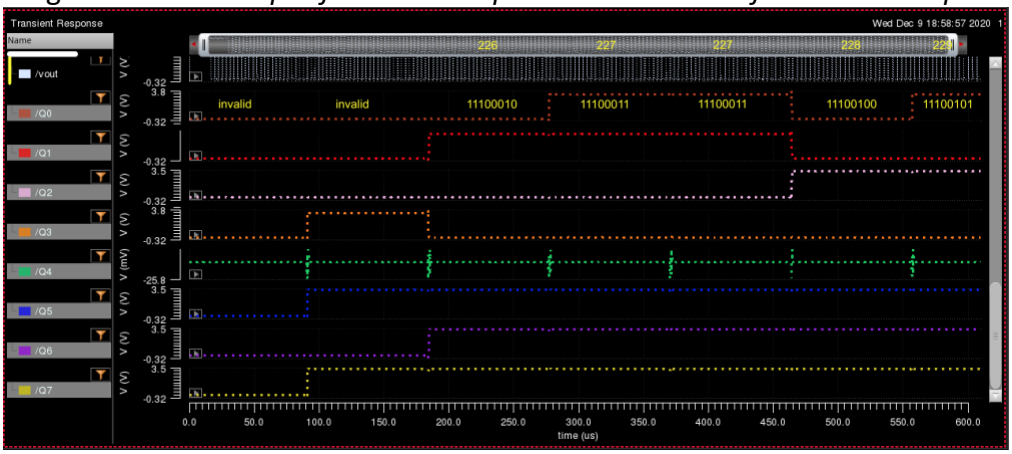


Figure 14. *ADC Output for Nonideal Sampler and Modulator for 2.9 to 3V input*

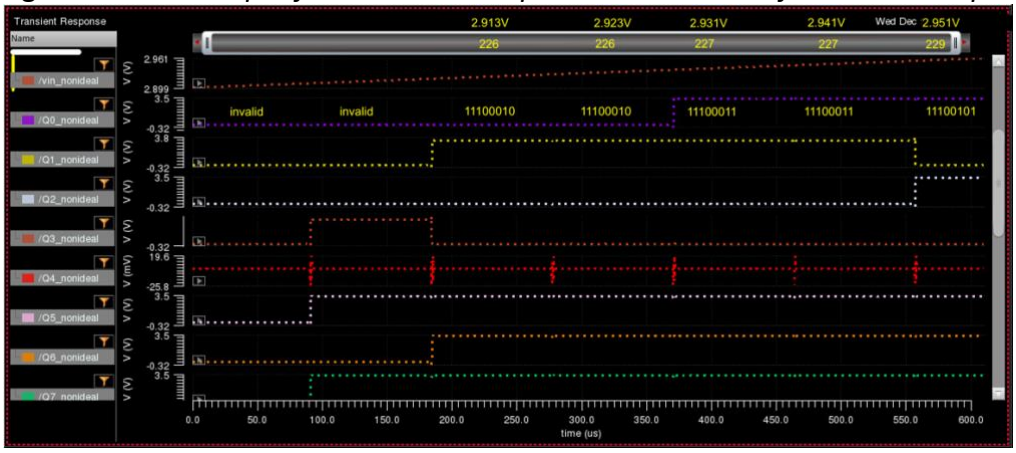


Figure 15. *Nonideal Modulator Signals (with vint ideal modulator signal)*

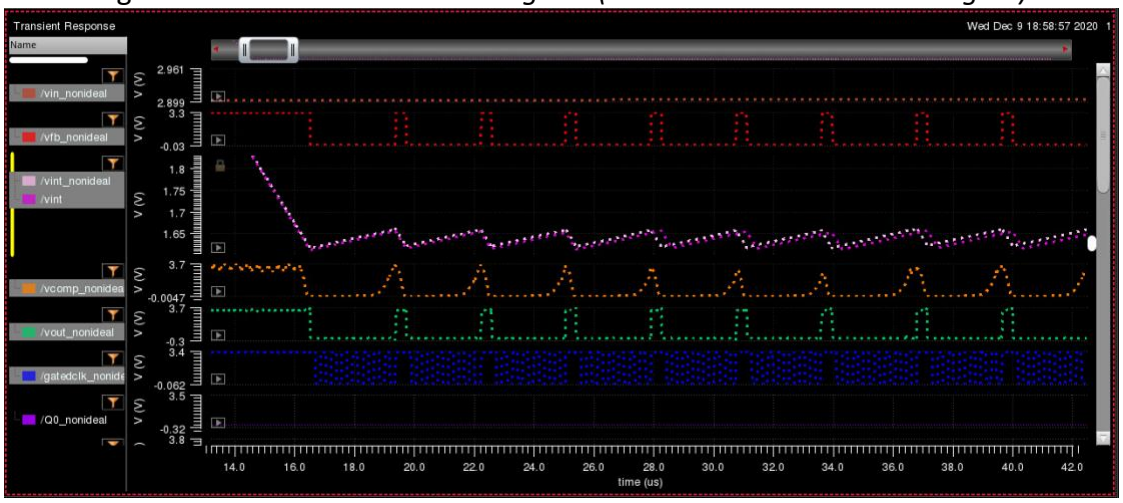


Figure 16. *ADC Output for Nonideal Sampler and Modulator with 0.9 to 1V ramp input*

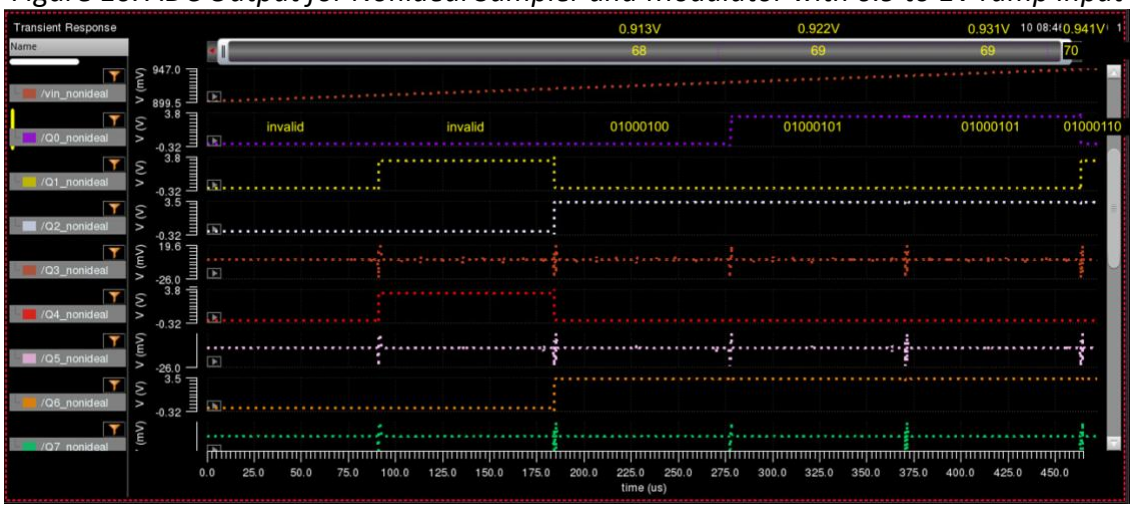
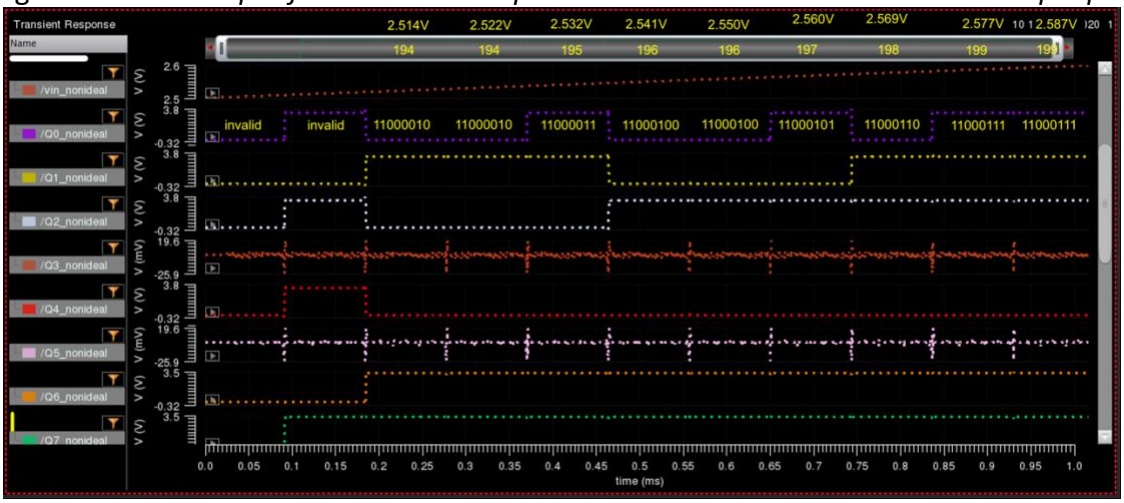


Figure 17. *ADC Output for Nonideal Sampler and Modulator with 2.5 to 2.6V ramp input*



Calculations

The integral nonlinearity (INL) and differential nonlinearity (DNL) values for the ADC for each of the ramp tests are calculated in Table 2. Optimally, the ADC's response to a ramp from 0V to 3.3V would have been used to calculate INL and DNL, but due to the long amount of time it took for a simulation to run (>20 mins), responses to shorter ramps were recorded and used instead.

This ADC has V_{FS} = 3.3V and N = 8. Therefore, by Equation 1, q = 0.013V.

The first two columns of Table 2 are the raw decimal outputs of the ADC (Q7 through Q0) in binary and volts (V_{actual} = Decimal output (V) = q*decimal output (decimal)). The third column is the average analog input that corresponds to the decimal output of the ADC (V_{ideal}). The fourth column uses Equation 8 to calculate raw INL values.

$$INL = V_{actual} - V_{ideal} \quad (8)$$

In order to remove the ADC's offset error, the INL of the first code for each ramp response was subtracted from V_{actual} in column 6 to calculate an offset-adjusted output (V_{actual}, adjusted). This V_{actual}, adjusted was then used in Equation 8 to calculate offset-adjusted INL (INL, adjusted) in column 7. DNL values were calculated in column 8 using Equation 9 and V_{actual}, adjusted.

$$DNL[i] = V_{actual}[i+1] - V_{actual}[i] - q \quad (9)$$

Around half of the ADC values have a DNL that is so small that it rounds down to 0, while another half has a DNL ≈ q. Since having a DNL greater than or equal to q can lead to a skipped code, this ADC has a significant amount of DNL which may lead to inaccuracies in analog-to-digital conversion. INL and DNL could have been reduced by correcting for ADC gain (slope) error, but this was difficult to correct for given that the ramps did not start at zero, so correction was more complicated than just multiplying by $V_{FS}/(V_{actual,\ max})$.

Table 2. *DNL and INL Calculations*

Ramp	Decimal output (Binary)	V_{actual} (V)	V_{ideal} (V)	INL, non-adjusted (V)	V_{actual}, adjusted (V)	INL, adjusted (V)	DNL (V)
2.9V to 3V	11100010	2.925	2.913	0.0117	2.9130	0.0000	-0.0129
	11100010	2.925	2.923	0.0017	2.9130	-0.0100	0.0000
	11100011	2.938	2.931	0.0066	2.9259	-0.0051	-0.0129
	11100011	2.938	2.941	-0.0034	2.9259	-0.0151	0.0129
	11100101	2.964	2.951	0.0125	2.9518	0.0008	
0.9V to 1V	1000100	0.880	0.913	-0.0330	0.9130	0.0000	0.0000
	1000101	0.893	0.922	-0.0291	0.9259	0.0039	-0.0129
	1000101	0.893	0.931	-0.0381	0.9259	-0.0051	0.0000
	1000110	0.906	0.941	-0.0351	0.9389	-0.0021	
2.5V to 2.6V	11000010	2.511	2.514	-0.0034	2.5140	0.0000	-0.0129
	11000010	2.511	2.522	-0.0114	2.5140	-0.0080	0.0000
	11000011	2.524	2.531	-0.0075	2.5269	-0.0041	0.0000
	11000100	2.536	2.541	-0.0045	2.5399	-0.0011	-0.0129

	11000100	2.536	2.55	-0.0135	2.5399	-0.0101	0.0000
	11000101	2.549	2.56	-0.0106	2.5528	-0.0072	0.0000
	11000110	2.562	2.569	-0.0066	2.5658	-0.0032	0.0000
	11000111	2.575	2.577	-0.0017	2.5787	0.0017	-0.0129
	11000111	2.575	2.587	-0.0117	2.5787	-0.0083	

IV. Layout Estimates

Analog Sampler and Modulator

This part of the area estimate evaluates the layout area for the ADC's sampler and delta-sigma modulator and includes all of the analog components in the ADC.

The lengths of all of the transistors in the op-amps are all 1 µm. There are 8 PMOS devices (6 with 0.5 µm width, and 2 with 2.8 µm width) and 6 NMOS devices (2 with 15 µm width and 4 with 0.5 µm width). The total active/gate area of these devices is the sum of all of the transistors' lengths*widths = 40.6 μm^2. This area can be multiplied by a factor of two to account for contacts and wiring, resulting in a rough estimate of total layout area of around 81.2 μm^2. It is important to note that each op amp requires a 5µA current source as well, which has not been accounted for in this area.

The area occupied by a capacitor corresponds to the capacitance required and a typical value for this correspondence is 2 fF/μm^2. Therefore, the 1nF capacitor requires 1*10^-9 /(2*10^-15) μm^2 = 500000 μm^2, while the 1nF capacitor requires 1.7*10^-12 /(2*10^-15) μm^2= 850 μm^2.

Resistors also occupy an area dependent on their desired resistance; this correspondence can be quantified to around 100 to 1000 Ohms per square. For the 15MΩ resistors, this means that the length of the resistive element must be 15MΩ*(squares/1000 Ω) = 15000 times its width. The minimum width for the resistive element is around 0.5 µm, making its required length 7500 µm, resulting in a total area of 3750 μm^2. This area may be larger if the resistive material is "snaked" to reduce the length of the resistor (trading off increased width for shorter length). For the current limiting 1Ω resistors, the length does not need to be extremely large to create 1Ω of resistance, causing the area that they occupy to be negligible.

The transistor pair used in the sampling circuit was allotted 20 x 3 μm^2 because they occupy an area roughly equivalent to an inverter (sized in the previous section).

As recorded in Table 3, the total area of the analog components is estimated to be 515,991 μm^2.

Table 3. *Analog Area Estimate*

Element	Description	Estimated Area (μm^2)	Number in Schematic
Op-amp	14 transistors 8 PMOS, 6 NMOS	81	3
Sampling Capacitor	1nF	500000	1
Integrator Capacitor	1.7pF	850	1
Integrator Resistor	15 MΩ	7500	2
Current limiting Resistor	1Ω	Negligible	8
Transistor pair	2 transistors	20 x 3	1

	1 PMOS, 1 NMOS		
TOTAL		**515,991**	

Digital Converter

For the ADC's digital converter, I made broad layout area estimates based off of each part's required number of transistors and widths and lengths. I included the modulator's D-Flip flop in the digital converter for ease of calculation.

The most basic building blocks for the digital logic components included inverters, 2-input NAND gates, and 3-input NAND gates. The inverter (Figure 6) was composed of 1 PMOS and 1 NMOS transistor with lengths of 2 µm and widths of 10 µm and 5 µm, respectively. The total width of the inverter was estimated to be >15 µm = 20 µm, and the length >2 µm = 3 µm. The 2-input NAND gate (Figure 6) was composed of 4 transistors with lengths of 2 µm and all widths equal to 5 µm. Its total width was estimated to be > 5 + 5 µm = 20 µm, and length > 2*2 µm = 6 µm. The 3-input NAND gate (Figure 6) was composed of 3 PMOS and 3 NMOS transistors with lengths of 2 µm and widths of 5 µm and 7.5 µm, respectively. The total width was estimated to be > 7.5 + 5 µm = 20 µm, and length > 3*2 µm = 9 µm. The widths of both NAND gates were overestimated to 20um such that the same VDD and GND rails could be used for the NAND gates and the inverter.

The D-Flip Flop area was estimated by summing the area of its composite parts (NAND gates and inverters). All parts were constrained to 1 VDD/GND rail set, such that the total D-Flip Flop width was 20 µm. The D-Flip Flop length was 3 µm/inverter*2 inverters + 6 µm/NAND*18 NANDs = 54 µm. The J-K Flip Flop area was estimated in a similar manner. All parts were constrained to 1 VDD/GND rail set, such that the total J-K Flip Flop width was 20 µm. The D-Flip Flop length was 3 µm/inverter*1 inverters + 6 µm/2-input NAND*5 2-input NANDs + 9 µm/3-input NAND*3 3-input NANDs = 60 µm.

The counters were assumed to be collections of stacked J-K flip flops, with each flip-flop sharing exactly 1 VDD or GND rail with the flip flop directly below it. Thus, the 8-bit counter had an estimated area of (20*8) µm x 60 µm and the 9-bit counter had an estimated area of (20*9) µm x 60 µm. Similarly, the register was assumed to be a collection of stacked D-Flip Flops, with each flip-flop sharing exactly 1 VDD or GND rail with the flip flop directly below it. The 8-bit register therefore had an estimated area of (20*8) µm x 54 µm.

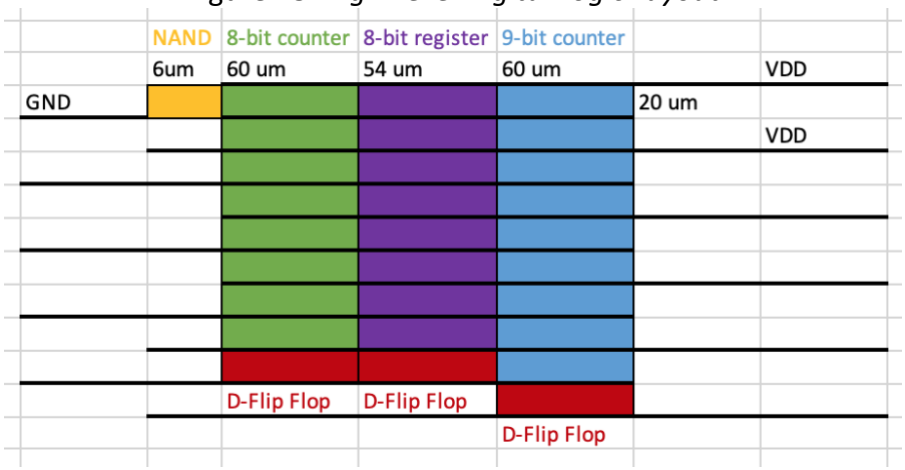
When placed together, the digital logic occupies an area of 200 µm x 180 µm (Figure 18). Note that the D-Flip flops occupy 20x54 μm^2, and do not always take up the entire space allotted for them. The area estimates are recorded in Table 4.

Table 4. *Digital Logic Area Estimate*

Element	Components	Estimated Area (μm^2)	Number in Schematic
Inverter	Transistors	20 x 3	
2-input NAND	Transistors	20 x 6	1
3-input NAND	Transistors	20 x 9	
D-Flip Flop	2-input NAND, Inverter	20 x 54	3

J-K Flip Flop	2-input NAND, 3-input NAND, Inverter	20 x 60	
8-bit counter	J-K Flip Flops	160 x 60	1
9-bit counter	J-K Flip Flops	180 x 60	1
8-bit register	D-Flip Flop	160 x 54	1
TOTAL		**200 x 180 = 36000**	

Figure 18. *High-Level Digital Logic Layout*



V. Power Estimate

The average power was estimated over 2 clock cycles of the ADC by running a transient simulation and then using the calculator function in Cadence to multiply each source's supplied voltage and currents over time and take the average. For these measurements, a full-scale 7.2kHz sinusoid was applied to the input of the ADC. The results of this estimation are shown below in Table 5. The total power consumed by the ADC is roughly 3.41*10^-4 W.

Table 5. *Power Consumption Estimate*

Current or Voltage Source	Average Power Consumed (W)
slowclk	3.38E-07
clknot	2.07E-07
clk	1.30E-06
gndv	4.95E-10
vdd	2.84E-04
vb1	3.95E-11
vb2	1.59E-10
vint_nonideal	3.71E-06
vfb_nonideal	1.46E-06
vcomp_nonideal	3.80E-06
vin_nonideal	4.57E-05
Total Power	**3.41E-04**

VI. Future Directions

The primary next step in this project would be to perform layouts for the entire ADC. Some next steps for the analog sampler/modulator section of the ADC could be to use different sampling or integrating circuits or to use a transistor network to generate the clocks. Firstly, a switched capacitor sampling circuit could be implemented instead of the sample-and-hold circuit to reduce error caused by charge injection. Secondly, since a significant part of the area of the sampler and modulator is attributed to the 2 15MΩ resistors in the integrator, a switched capacitor circuit could replace the current R-C integrator such that these resistors are no longer needed. Lastly, generating inverted and noninverted clocks with the same delay would involve feeding the clock into 2 branches of a circuit: a pass transistor gate and an inverter, such that the delay through each would be the same. The output of the pass transistor gate would be clk and the output of the inverter would be clknot.

One future direction for the digital logic section of the ADC could be to use a counter to generate the slowclk signal from clk. For ease of testing and due to project time constraints, slowclk is currently generated using a vpulse instance. However, since slowclk has twice the period of clk, it could be generated by feeding clk into a counter and using the LSB of that counter as slowclk.